CLAIMS

What is claimed is:

1. A method for increasing the strength of an electroplating cathode contact area on a semiconductor wafer comprising the steps of:

providing a semiconductor wafer comprising a periphery portion and a central portion said central portion comprising at least one insulating layer including a plurality of etched openings in closed communication with an underlying conductive area for filling with metal to form interconnecting conductive pathways;

forming a metal seed layer over the central portion;

providing a plurality of cathode contact areas within the periphery portion of the semiconductor wafer said cathode contact areas comprising a cathode contact area insulating layer including a plurality of cathode contact area etched openings in closed communication with an underlying conductive region in electrical communication with the metal seed layer;

filling the of cathode contact area etched openings with metal to form cathode contact area metal interconnects in electrical communication with the underlying conductive region;

planarizing an exposed surface of the cathode contact area metal interconnects; and

forming a conductive layer over the cathode contact area metal interconnects to form a plurality of cathode contact pads for contacting a cathode for carrying out an electroplating process.

2. The method of claim 1, further comprising the step prior to the filling step of depositing a barrier layer to cover at least the cathode contact area etched opening sidewalls and floors.

3. The method of claim 2, wherein the barrier layer includes tantalum, tantalum nitride, titanium nitride, and combinations thereof.

4. The method of claim 1, wherein the metal seed layer, the cathode contact area metal interconnects, and the contact pads comprise copper or an alloy thereof.

5. The method of claim 1, wherein the cathode contact area metal interconnects comprise at least one of vias and trench lines.

6. The method of claim 1, wherein the cathode contact area insulating layer comprises an insulating layer with a dielectric constant of less than about 3.0.

7. The method of claim 1, wherein the cathode contact pads form a rectangular area from about 50 microns to about 150 microns on a side.

8. The method of claim 1, wherein the periphery portion is disposed along a circumferential edge of the semiconductor wafer.

9. The method of claim 8, wherein the circumferential edge of the semiconductor wafer toward the central portion by a radial distance ranges between about 1mm to about 3mm.

10. The method of claim 9, wherein the plurality of cathode contact pads are disposed to include the entire circumference of the semiconductor wafer.

11. A method for forming electroplating cathode contacts around the periphery of a semiconductor wafer comprising the steps of:

forming an insulating layer over a conductive layer extending at least around the periphery of a semiconductor wafer substrate;

etching a plurality of openings around a peripheral portion of the semiconductor wafer substrate through the insulating layer to extend through a thickness of the insulating layer in closed communication with the conductive layer said conductive area in electrical communication with a central portion of the semiconductor wafer substrate;

filling the plurality of openings with metal to form electrically conductive pathways;

planarizing the electrically conductive pathway surfaces; and

forming a metal layer over the electrically conductive pathway surfaces to form a plurality of contact pads for contacting a cathode for carrying out an electroplating process.

12. The method of claim 11, further comprising the step prior to the filling step of depositing a barrier layer to cover at least sidewalls and floors within the plurality of openings.

13. The method of claim 12, wherein the barrier layer includes tantalum, tantalum nitride, titanium nitride, and combinations thereof.

14. The method of claim 11, wherein the conductive pathways and the plurality of contact pads are selected from the group consisting of copper, aluminum, and tungsten.

15. The method of claim 11, wherein the conductive pathways comprise at least one of vias and trench lines.

16. The method of claim 11, wherein the conductive pathways comprise a mixture of vias and trench lines.

17. The method of claim 11, wherein the insulating layer comprises an insulating layer with a dielectric constant of less than about 3.0.

18. The method of claim 11, wherein an individual contact pad forms a rectangular area from about 50 microns to about 150 microns on a side.

19. The method of claim 11, wherein the plurality of contact pads are disposed within a region extending along a circumferential edge of the semiconductor wafer.

20. The method of claim 11, wherein the electroplating process is performed on a central portion of the semiconductor wafer including a metal seed layer.